SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application is based upon and claims the benefit of priority from the prior Japanese Patent Application No. 2002-255473, filed on Aug. 30, 2002, the entire contents of which are incorporated herein by reference.

FIELD OF THE INVENTION

[0002] The present invention relates to a semiconductor device such as a MOS transistor having a gate, a source, and a drain, and a method for manufacturing the same.

DESCRIPTION OF THE RELATED ART

[0003] Recently, along with progress in high integration and high performance for a semiconductor device, various demands for the semiconductor device have been still more increasing. Among them, strong demands are to make even thinner films of a gate insulation film and a sidewall insulation film. This causes to increase fringe capacitance, that is, parasitic capacitance generated mainly between a gate electrode and a semiconductor substrate, which is seen as a problem. As a conventional art to attempt reducing this fringe capacitance, for example, Japanese Patent Laid-open No. Hei 9-246544 discloses technology to provide a cavity on a whole side surface between the gate electrode and the gate insulation film and the sidewall insulation film.

[0004] The above-described conventional art is effective to a great extent in reducing the fringe capacitance, but then in the first place, forming the cavity is not a simple task, and further an impurity introduced into the gate electrode in order to facilitate threshold voltage control tends to escape from the cavity in heat treatment processes thereafter.

SUMMARY OF THE INVENTION

[0005] An object of the present invention is to provide such a semiconductor device as to reduce fringe capacitance in the most effective manner and to deter an escape of the above-mentioned impurity as much as possible, as well as to have a relatively simple manufacturing, and to provide a method for manufacturing the same.

[0006] The inventor reaches various aspects of the present invention described below through a committed consideration.

[0007] This invention aims at a semiconductor device including a gate, a source, and a drain, and a method for manufacturing the same.

[0008] A semiconductor device according to this invention has: a sidewall film covering a side surface of the gate; and a low permittivity region locally provided only at a lower portion of the side surface of the gate with the low permittivity region being covered by the sidewall film. The low permittivity region is preferably filled with a predetermined low permittivity material or left as a cavity.

[0009] A method for manufacturing the semiconductor device according to this invention includes the steps of: forming a thin first film covering a side surface of the gate; removing only a lower portion of the first film; locally filling only a lower portion of the side surface of the gate, at which the first film is removed, with a lower permittivity material as compared to the first film; and forming a second film on the first film to cover the low permittivity material.

[0010] A method for manufacturing the semiconductor device according to this invention includes the steps of: forming a thin first film covering a side surface of the gate; removing only a lower portion of the first film; and forming a second film on the first film with low step coverage, to thereby form a cavity at a lower portion of the side surface of the gate.

[0011] A method for manufacturing the semiconductor device according to this invention includes the steps of: removing a part of a side wall lower portion of the gate to process it into a notched shape; locally filling only the part with a lower permittivity material as compared to the first film; and forming a sidewall film on a side surface of the gate to cover the low permittivity material.

[0012] A method for manufacturing the semiconductor device according to this invention includes the steps of: removing a part of a side wall lower portion of the gate to process it into a notched shape; and forming a sidewall film on a side surface of the gate with low step coverage to such an extent as not to fill in the part, to thereby form a cavity at a lower portion of the side surface of the gate.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] **FIG. 1** is a schematic sectional view to describe a first aspect of this invention;

[0014] **FIG. 2** is a schematic sectional view to describe a second aspect of this invention;

[0015] **FIG. 3** is a schematic sectional view to describe a third aspect of this invention;

[0016] **FIG. 4** is a schematic sectional view to describe a fourth aspect of this invention;

[0017] **FIGS. 5A** to **5**G are schematic sectional views showing, in a process order, a method for manufacturing a MOS transistor relating to a first embodiment;

[0018] **FIG. 6A** to **6**F are schematic sectional views showing, in a process order, a method for manufacturing a MOS transistor relating to a second embodiment;

[0019] **FIG. 7A** to **7**F are schematic sectional views showing, in a process order, a method for manufacturing a MOS transistor relating to a third embodiment;

[0020] **FIG. 8A** to **8**E are schematic sectional views showing, in a process order, a method for manufacturing a MOS transistor relating to a fourth embodiment, and

[0021] **FIG. 9** is a characteristic chart showing the relation between height of a low permittivity region (cavity) and fringe capacitance in the MOS transistor relating to the second embodiment.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0022] Main Points of the Present Invention

[0023] In an attempt to reduce fringe capacitance, the inventor of the present invention adds a point of deterring an